REMARKS

This Amendment is filed in response to the Office Action dated May 16, 2005, which has a shortened statutory period set to expire August 16, 2005.

Rejections Under 35 U.S.C. 103

Claims 1, 3, 4, 6, 8-10, 12, and 14-17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Okada in view of Manohar. Applicant respectfully traverses this rejection in light of the following remarks.

Claim 1 recites:

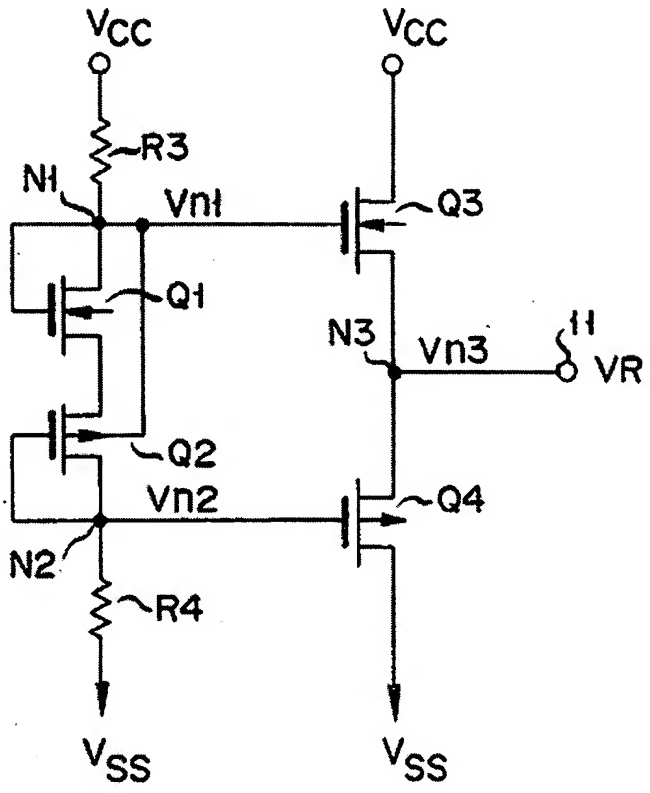
> **A current mirror** comprising:
>
> **a first transistor of a first conductivity type**, the first transistor being diode-connected;
>
> **a second transistor of a second conductivity type**, a **drain of the second transistor being connected to a drain** of the first transistor, and **a gate of the second transistor being connected to a source** of the first transistor;
>
> **a third transistor of the first conductivity type**, a gate of the third transistor being connected to a gate of the first transistor; and
>
> **a fourth transistor of the first conductivity type**, a gate of the fourth transistor being connected to a source of the second transistor. (Emphasis added.)

A transistor configuration as recited by Claim 1 beneficially allows a current mirror to exhibit an "output impedance [that] is substantially similar to that of [a] Wilson current mirror." (Specification, paragraph 45.)

The Office Action states that FIG. 4 of Okada teaches "a current mirror circuit, first transistor (Q1), second transistor (Q2), third transistor (Q3) and fourth transistor (Q4)." Applicant respectfully submits that this is an improper interpretation of Okada.

FIG. 4 of Okada (duplicated here for reference) is "an intermediate potential generation circuit". (Okada, col. 3, lines 43-44.) As noted by Okada, "an intermediate potential generation circuit ... generates an intermediate potential from a power source voltage applied to the device." (Okada, col. 1, lines 6-10.) Therefore, Okada certainly does not teach "[a] current mirror" as recited by Claim 1, particularly in light of the stated intent of Okada to provide "an intermediate potential generation circuit with **low current consumption and large current driving power.**" (Okada, col. 1, lines 44-46, emphasis added.)

F I G. 4



However, even assuming, arguendo, that FIG. 4 of Okada can be considered a current mirror, Okada still does not disclose or suggest "a second transistor of a second conductivity type, a **drain of the second transistor being connected to a drain** of the first transistor, and a **gate of the second transistor being connected to a source** of the first transistor" (emphasis added) as recited by Claim 1. The Office Action indicates that transistors Q1 and Q2 of Okada correspond to the "first transistor" and the "second transistor", respectively, recited by Claim 1, thereby indicating that the drain of transistor Q1 should be connected to the drain of transistor Q2, and that the gate of transistor Q2 should be connected to the source of transistor Q1. However, as is clearly depicted in FIG. 4 of

Okada, the **source** of n-channel transistor Q1 is connected to the **source** of p-channel transistor Q2. Furthermore, the gate of transistor Q2 is connected to the source of transistor Q2, and is **not** connected to "a source of **the first transistor**" (emphasis added) as recited by Claim 1. In fact, no combination of transistors Q1 through Q4 in FIG. 4 of Okada (or in any other figure of Okada) exhibits the configuration recited by Claim 1.

Furthermore, FIG. 4 of Okada does not show "a first transistor of a **first conductivity** type, ... a second transistor of a **second conductivity** type, ... a third transistor of the **first conductivity** type, ... and a fourth transistor of the **first conductivity** type" (emphasis added) as recited by Claim 1. FIG. 4 of Okada clearly depicts two n-channel transistors (Q1 and Q3) and two p-channel transistors (Q2 and Q4). In fact, every figure of Okada depicts the same two n-channel transistors and two p-channel transistors.

Manohar teaches a voltage reference circuit and does not remedy any of the above-described deficiencies of Okada. The Office Action seems to indicate that because Manohar mentions that circuits can be implemented using PMOS or NMOS devices, and because Manohar also mentions a current mirror circuit, that the transistors in FIG. 4 of Okada can be changed from p-type to n-type, and vice-versa, to allow that circuit to match the recited configuration of Claim 1. However, applying such switching to Okada would actually render the circuit of Okada inoperable. For example, replacing n-channel transistor Q1 with a p-channel transistor would result in a gate-source coupled p-channel transistor that would always be off. Similarly, replacing p-channel transistor Q2 with an n-channel transistor would also result in a constantly off transistor (i.e., a gate-source coupled n-channel transistor).

Thus, for at least these reasons, Claim 1 is allowable

under 35 U.S.C. 103(a) over Okada in view of Manohar. Claims 3, 4, and 6 depend from Claim 1, and are therefore allowable over Okada in view of Manohar for at least the same reasons that Claim 1 is allowable. Accordingly, Applicant respectfully requests reconsideration and allowance of Claims 1, 3, 4, and 6.

Claim 3 recites "wherein the first transistor, the second transistor, the third transistor, and the fourth transistor are matched transistors". In contrast, Okada states that the "**[c]hannel widths W3 and W4** of MOS transistors Q3 and Q4 are **set to be larger than channel widths W1 and W2** of MOS transistors Q1 and Q2." (Okada, col. 2, lines 51-53, emphasis added.) Manohar does not remedy this deficiency of Okada. Therefore, for at least this additional reason, Claim 3 is further allowable over Okada in view of Manohar.

Claim 8 recites:

> A method for generating an output current, the method comprising:
>
> **providing a reference current** to a diode-connected transistor **via a saturated transistor**, wherein the diode-connected transistor and the saturated transistor have different conductivity types;
>
> providing a gate voltage of the diode-connected transistor to a mirroring transistor to generate an output current;
>
> providing the output current to an output terminal via an output transistor; and
>
> providing **a source voltage of the saturated transistor to a gate** of the output transistor. (Emphasis added.)

In FIG. 4 of Okada, both transistors Q1 and Q2 are gate-drain coupled, and hence, both transistors Q1 and Q2 are diode-connected transistors. Therefore, neither transistor is "a saturated transistor" as recited by Claim 8. Furthermore, even assuming, arguendo, that one of transistors Q1 and Q2 could be considered a saturated transistor, nowhere does Okada disclose

or suggest "providing a reference current" as recited in Claim 1, to either of transistors Q1 or Q2. The current flow through transistors Q1 and Q2 depends not only on the values of resistors R3 and R4, but also on the threshold voltages of transistors Q1 and Q2, which by definition means that a **reference current** is **not** being provided to either transistor Q1 or Q2.

In addition, Okada does not teach "providing **a source voltage of the saturated transistor to a gate** of the output transistor," (emphasis added) as recited by Claim 8. As noted above, nowhere does Okada teach a saturated transistor. Furthermore, no transistor in FIG. 4 of Okada is coupled to receive the source voltage from any other transistor in FIG. 4. For reasons substantially similar to those described above with respect to Claim 1, Manohar does not remedy these deficiencies of Claim 8.

Thus for at least these reasons, Claim 8 is allowable under 35 U.S.C. 103(a) over Okada in view of Manohar. Claims 9, 10, and 12 depend from Claim 8, and are therefore allowable over Okada in view of Manohar for at least the same reasons that Claim 8 is allowable. Accordingly, Applicant respectfully requests reconsideration and allowance of Claims 8-10 and 12.

Claim 9 recites "wherein the diode-connected transistor, the saturated transistor, the mirroring transistor, and the output transistor are **all matched transistors**." (Emphasis added.) In contrast, Okada states that the "**[c]hannel widths W3 and W4** of MOS transistors Q3 and Q4 are **set to be larger than channel widths W1 and W2** of MOS transistors Q1 and Q2." (Okada, col. 2, lines 51-53, emphasis added.) Manohar does not remedy this deficiency of Okada. Therefore, for at least this additional reason, Claim 9 is further allowable over Okada in view of Manohar.

Claim 14 recites:

> A method for providing an output current, the method comprising:
>
> cascoding a first transistor and a second transistor **between an output terminal and a first supply voltage;**
>
> **supplying a reference current** to a third transistor via a fourth transistor, the third transistor being diode-connected, the third transistor and the fourth transistor having different conductivity types;
>
> **providing the first supply voltage to a gate of the fourth transistor;**
>
> providing a gate voltage of the third transistor to a gate of the second transistor; and
>
> **providing a source voltage of the fourth transistor to a gate** of the first transistor.
>
> (Emphasis added.)

As noted above with respect to Claim 8, Okada does not teach "supplying a reference current" and "providing a source voltage of the fourth transistor to a gate of the first transistor" as recited by Claim 14. Manohar does not remedy these deficiencies of Okada.

Furthermore, as shown in FIG. 4 of Okada, Okada does not teach "cascoding a first transistor and a second transistor between an output terminal and a first supply voltage" as recited by Claim 14. Instead, Okada teaches an output terminal (11) at the junction of transistors Q3 and Q4. In addition, Okada does not teach "providing the first supply voltage to a gate of the fourth transistor" as recited by Claim 14, since none of transistors Q1 through Q4 in FIG. 4 of Okada is coupled to receive a supply voltage. Transistors Q1 and Q2 receive gate voltages that are offset from supply voltages Vcc and Vss, respectively, by the voltage drops across resistors R3 and R4, respectively. Once again, Manohar does not remedy these deficiencies of Okada.

Thus, for at least these reasons, Claim 14 is allowable

under 35 U.S.C. 103(a) over Okada in view of Manohar. Claims 15-17 depend from Claim 14, and are therefore allowable over Okada in view of Manohar for at least the same reasons that Claim 14 is allowable. Accordingly, Applicant respectfully requests reconsideration and allowance of Claims 14-17.

Claim 15 recites " wherein the first transistor, the second transistor, the third transistor, and the fourth transistor comprise **matched transistors**." (Emphasis added.) In contrast, Okada states that the "**[c]hannel widths W3 and W4** of MOS transistors Q3 and Q4 are **set to be larger than channel widths W1 and W2** of MOS transistors Q1 and Q2." (Okada, col. 2, lines 51-53, emphasis added.) Manohar does not remedy this deficiency of Okada. Therefore, for at least this additional reason, Claim 15 is further allowable over Okada in view of Manohar.

Allowable Subject Matter

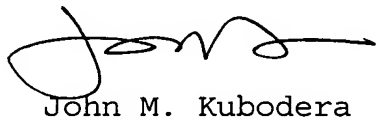
The Office Action states that Claims 2, 5, 7, 11, and 13 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening Claims. Applicant notes with appreciation the Examiner's recognition of allowable subject matter in those claims. However, because Applicant believes that independent Claim 1, from which Claims 2, 5 and 7 depend, and independent Claim 8, from which Claims 11 and 13 depend, are allowable for the reasons presented above, Claims 2, 5, 7, 11, and 13 are not amended in the present paper.

CONCLUSION

Claims 1-17 are pending in the present Application. Allowance of these claims is respectfully requested.

If there are any questions, please telephone the undersigned at 408-451-5903 to expedite prosecution of this case.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 16, 2005.

8/16/2005 Rebecca A. Baumann
Date Signature: Rebecca A. Baumann